Course Title	**Digital Logic Design**		
Course Code	**CSC-315**		
Credit Hours	3 (3,0)		
Category	Computer Science Core		
Prerequisite	None		
Co-Requisite	None		
Follow Up	CSC-215 Computer Organization & Architecture (Assembly language included)		
Course Introduction	The course introduces the concept of digital logic, gates and the digital circuits. Further, it focuses on the design and analysis combinational and sequential circuits. It also serves to familiarize the student with the logic design of basic computer hardware components.		
Course Learning Outcomes (CLOs)	At the end of the course, the students will be able to:	**BT**	**PLO**
	CLO1: Draw and interpret digital logic diagrams, including combinational and sequential circuits.	C2 (Understand)	1, 2, 3
	CLO 2: Design basic digital components such as multiplexers, flip-flops, and encoders.	C6 (Create)	1,3,4,5
	CLO 3: Analyze the behaviour of digital systems using truth tables and Boolean algebra.	C4 (Analyze)	3
	CLO 4: Implement simple digital circuits using logic gates.	C3 (Apply)	4, 5
	CLO 5: Understand the fundamentals of digital system design and their applications.	C2 (Understand)	1,2,8,10
Text Book(s)	1. M. Morris Mano, Digital Logic and Computer Design, 1st Edition, Pearson, 1979, ISBN:0132145103.		
Reference Material	1. Thomas L. Floyd, Digital Fundamentals, 10th Edition, Prentice Hall, 2008, ISBN: 0132359235. 2. Fundamental of Digital Logic with Verilog Design, Stephen Brown, 2/e		

Weekly Lesson Plan

Week No.	Course Content	Assignments/Readings
Week 1	Introduction to Digital Systems, Number Systems (base conversions, data encodings , radix and diminished radix complements and applying in subtraction)	Mano: Chapter 1
Week 2	Introduction to Boolean Algebra, Basic theorems and properties of Boolean Algebra,	Mano: Chapter 2 Quiz 1
Week 3	Boolean Functions. Canonical Forms (Representation of Function in Sum of Minterms or Product of Maxterms,), Standard Forms.	Mano: Chapter 2 Assignment 1
Week 4	Simplification of Boolean function using Boolean Algebra	Mano: Chapter 2
Week 5	Logic Gates, NAND and NOR Implementation,	Mano: Chapter 2 Quiz 2
Week 6	Simplification of Boolean function using Karnaugh Map,	Mano: Chapter 3 Assignment 2
Week 7	Don’t care Conditions in K Maps	Mano: Chapter 3

Week 8	The Tabulation Method	Mano: Chapter 3 Quiz 3
Week 9	Introduction to Combinational Logic, Design of Adders, Design of Subtractors, Code Convertors, Analysis Procedure of Combinational Circuits	Mano: Chapter 4 Assignment 3
Week 10	Binary Parallel Adders, Decimal Adders, Magnitude Comparator, Decoders and its applications, Multiplexers, Demultiplexers, Encoders, ROM, Programmable Logic Array (PLA),	Mano: Chapter 5
Week 11	Introduction to Sequential Circuits, Basic Flip Flop, Clocked RS Flip Flop, Clocked D Flip Flop, Clocked JK Flip Flop, Clocked T Flip Flop,	Mano: Chapter 6 Quiz 4
Week 12	Analysis of Clocked Sequential Circuits, State Reduction and Assignment,	Mano: Chapter 6 Assignment 4
Week 13	Introduction to Registers, Shift Registers, Ripple Counters, Synchronous Counters , Timing Sequences	Mano: Chapter 7
Week 14	Memory Unit, Random Access Memory	Mano: Chapter 7 Quiz 5
Week 15	Introduction Programmable Logic Devices	Mano: Chapter 7 Assignment 5
Week 16	Verilog HDL/VHDL, MultiSim Familiarization (or anyother SPICE Simulation Tool) SPICE: Simulation Program with Integrated Circuit Emphasis	Mano: Chapter 4 - 6